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2016 - 2017 VLSI IEEE FINAL YEAR Projects @ JP INFOTeCH

S.NO	Project Code	IEEE 2016-17 VLSI Project Titles	Domain	Lang/Year
1	JPV1601	A Fully Digital Front-End Architecture for ECG Acquisition System With 0.5 V Supply	LOW POWER	VLSI/2016
2	JPV1602	Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication	LOW POWER	VLSI/2016
3	JPV1603	RF Power Gating: A Low-Power Technique for Adaptive Radios	LOW POWER	VLSI/2016
4	JPV1604	Low-Power ECG-Based Processor for Predicting Ventricular Arrhythmia	LOW POWER	VLSI/2016
5	JPV1605	A New Parallel VLSI Architecture for Real-Time Electrical Capacitance Tomography	LOW POWER	VLSI/2016
6	JPV1606	Low-Power FPGA Design Using Memoization-Based Approximate Computing	LOW POWER	VLSI/2016
7	JPV1607	Low-Power Split-Radix FFT Processors Using Radix-2 Butterfly Units	LOW POWER	VLSI/2016
8	JPV1608	A High-Speed FPGA Implementation of an RSD-Based ECC Processor	HIGH SPEED DATA TRANSMISSION	VLSI/2016
9	JPV1609	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	HIGH SPEED DATA TRANSMISSION	VLSI/2016
10	JPV1610	A 0.52/1 V Fast Lock-in ADPLL for Supporting Dynamic Voltage and Frequency Scaling	HIGH SPEED DATA TRANSMISSION	VLSI/2016
11	JPV1611	Code Compression for Embedded Systems Using Separated	HIGH SPEED DATA	VLSI/2016

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		Dictionaries	TRANSMISSION	
12	JPV1612	A Dynamically Reconfigurable Multi-ASIP Architecture for Multi-standard and Multimode Turbo Decoding	HIGH SPEED DATA TRANSMISSION	VLSI/2016
13	JPV1613	Design and Implementation of High-Speed All-Pass Transformation-Based Variable Digital Filters by Breaking the Dependence of Operating Frequency on Filter Order	HIGH SPEED DATA TRANSMISSION	VLSI/2016
14	JPV1614	A Mixed-Decimation MDF Architecture for Radix-2^K Parallel FFT	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
15	JPV1615	Algorithm and Architecture of Configurable Joint Detection and Decoding for MIMO Wireless Communications With Convolution Codes	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
16	JPV1616	One-Cycle Correction of Timing Errors in Pipelines With Standard Clocked Elements	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
17	JPV1617	Hardware and Energy-Efficient Stochastic LU Decomposition Scheme for MIMO Receivers	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
18	JPV1618	Hybrid LUT/Multiplexer FPGA Logic Architectures	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
19	JPV1619	A 520k (18 900, 17 010) Array Dispersion LDPC Decoder Architectures for NAND-Flash Memory	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
20	JPV1620	Implementing Minimum-Energy-Point Systems With Adaptive Logic	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016

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21	JPV1621	High-Performance Pipelined Architecture of Elliptic Curve Scalar Multiplication Over GF(2^m)	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
22	JPV1622	High-Performance NB-LDPC Decoder With Reduction of Message Exchange	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
23	JPV1623	LUT Optimization for Distributed Arithmetic-Based Block Least Mean Square Adaptive Filter	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
24	JPV1624	Graph-Based Transistor Network Generation Method for Supergate Design	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
25	JPV1625	Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
26	JPV1626	A Cellular Network Architecture With Polynomial Weight Functions	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
27	JPV1627	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
28	JPV1628	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
29	JPV1629	Exploiting Intracell Bit-Error Characteristics to Improve Min-Sum LDPC Decoding for MLC NAND Flash-Based Storage in Mobile Device	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
30	JPV1630	Unequal-Error-Protection Error Correction Codes for the	AREA EFFICIENT/ TIMING & DELAY	VLSI/2016

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		Embedded Memories in Digital Signal Processors	REDUCTION	
31	JPV1631	A High Throughput List Decoder Architecture for Polar Codes	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
32	JPV1632	A Normal I/O Order Radix-2 FFT Architecture to Process Twin Data Streams for MIMO	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
33	JPV1633	Design and FPGA Implementation of a Reconfigurable 1024-Channel Channelization Architecture for SDR Application	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
34	JPV1634	Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding	Audio, Image and Video Processing	VLSI/2016
35	JPV1635	A Configurable Parallel Hardware Architecture for Efficient Integral Histogram Image Computing	Audio, Image and Video Processing	VLSI/2016
36	JPV1636	A New Binary-Halved Clustering Method and ERT Processor for ASSR System	Audio, Image and Video Processing	VLSI/2016
37	JPV1637	The VLSI Architecture of a Highly Efficient De-blocking Filter for HEVC Systems	Audio, Image and Video Processing	VLSI/2016
38	JPV1638	Low-Power System for Detection of Symptomatic Patterns in Audio Biological Signals	Audio, Image and Video Processing	VLSI/2016
39	JPV1639	In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers	NETWORKING	VLSI/2016
40	JPV1640	Source Code Error Detection in High-Level Synthesis Functional Verification	VERIFICATION	VLSI/2016
41	JPV1641	A Single-Ended With Dynamic Feedback Control 8T Subthreshold SRAM Cell	TANNER /MICROWIND – (AREA EFFICEINT)	VLSI/2016

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42	JPV1642	OTA-Based Logarithmic Circuit for Arbitrary Input Signal and Its Application	TANNER /MICROWIND – (AREA EFFICEINT)	VLSI/2016
43	JPV1643	A Robust Energy/Area-Efficient Forwarded-Clock Receiver With All-Digital Clock and Data Recovery in 28-nm CMOS for High-Density Interconnects	TANNER /MICROWIND – (AREA EFFICEINT)	VLSI/2016
44	JPV1644	Full-Swing Local Bitline SRAM Architecture Based on the 22-nm FinFET Technology for Low-Voltage Operation	TANNER /MICROWIND – (AREA EFFICEINT)	VLSI/2016
45	JPV1645	A 0.1–3.5-GHz Duty-Cycle Measurement and Correction Technique in 130-nm CMOS	TANNER /MICROWIND – (AREA EFFICEINT)	VLSI/2016
46	JPV1646	A Low-Power Robust Easily Cascaded PentaMTJ-Based Combinational and Sequential Circuits	TANNER /MICROWIND – (LOW POWER)	VLSI/2016
47	JPV1647	Low-Power Variation-Tolerant Nonvolatile Lookup Table Design	TANNER /MICROWIND – (LOW POWER)	VLSI/2016
48	JPV1648	Low-Energy Power-ON-Reset Circuit for Dual Supply SRAM	TANNER /MICROWIND – (LOW POWER)	VLSI/2016
49	JPV1649	Frequency-Boost Jitter Reduction for Voltage-Controlled Ring Oscillators	TANNER /MICROWIND – (LOW POWER)	VLSI/2016
50	JPV1650	High-Speed, Low-Power, and Highly Reliable Frequency Multiplier for DLL-Based Clock Generator	TANNER /MICROWIND – (LOW POWER)	VLSI/2016
51	JPV1651	A Systematic Design Methodology of Asynchronous SAR ADCs	TANNER /MICROWIND – (AREA EFFICEINT)	VLSI/2016
52	JPV1652	Read Bit line Sensing and Fast Local Write-Back Techniques in Hierarchical Bitline Architecture for Ultralow-Voltage SRAMs	TANNER /MICROWIND – (AREA EFFICEINT)	VLSI/2016
53	JPV1653	Online Measurement of Degradation Due to Bias Temperature Instability in SRAMs	TANNER /MICROWIND – (AREA EFFICEINT)	VLSI/2016

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55	JPV1655	EMDBAM: A Low-Power Dual Bit Associative Memory with Match Error and Mask Control	TANNER /MICROWIND – (LOW POWER)	VLSI/2016
56	JPV1656	A Single-Stage Low-Dropout Regulator With a Wide Dynamic Range for Generic Applications	TANNER /MICROWIND – (LOW POWER)	VLSI/2016
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59	JPV1659	Design of Silicon Photonic Interconnect ICs in 65-nm CMOS Technology	TANNER /MICROWIND – (LOW POWER)	VLSI/2016
60	JPV1660	Test Escapes of Stuck-Open Faults Caused by Parasitic Capacitances and Leakage Currents	TANNER /MICROWIND – (LOW POWER)	VLSI/2016
61	JPV1661	Statistical Framework and Built-In Self Speed-Binning System for Speed Binning Using On-Chip Ring Oscillators	HIGH SPEED DATA TRANSMISSION	VLSI/2016
62	JPV1662	A Low-Power Broad-Bandwidth Noise Cancellation VLSI Circuit Design for In-Ear Headphones	HIGH SPEED DATA TRANSMISSION	VLSI/2016
63	JPV1663	A 3-D CPU-FPGA-DRAM Hybrid Architecture for Low-Power Computation	LOW POWER	VLSI/2016
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65	JPV1665	Design of a Network of Digital Sensor Macros for Extracting Power Supply Noise Profile in SoCs	LOW POWER	VLSI/2016

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67	JPV1667	FCUDA-NoC : A Scalable and Efficient Network-on-Chip Implementation for the CUDA-to-FPGA Flow	NETWORKING	VLSI/2016
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71	JPV1671	Source Coding and Preemphasis for Double-Edged Pulse width Modulation Serial Communication	HIGH SPEED DATA TRANSMISSION	VLSI/2016
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73	JPV1673	Network-on-Chip for Turbo Decoders	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
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82	JPV1682	Energy-Efficient Floating-Point MFCC Extraction Architecture for Speech Recognition Systems	Audio, Image and Video Processing	VLSI/2016
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84	JPV1684	A Fast Fault-Tolerant Architecture for Sauvola Local Image Thresholding Algorithm Using Stochastic Computing	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
85	JPV1685	Efficiency Enablers of Lightweight SDR for MIMO Baseband Processing	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016

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89	JPV1689	An All-Digital Approach to Supply Noise Cancellation in Digital Phase-Locked Loop	HIGH SPEED DATA TRANSMISSION	VLSI/2016
90	JPV1690	Write Buffer-Oriented Energy Reduction in the L1 Data Cache for Embedded Systems	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
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97	JPV1697	Design of Modified Second-Order Frequency Transformations Based Variable Digital Filters With Large Cutoff Frequency Range and Improved Transition Band Characteristics	HIGH SPEED DATA TRANSMISSION	VLSI/2016
98	JPV1698	Fixed-Point Computing Element Design for Transcendental Functions and Primary Operations in Speech Processing	Audio, Image and Video Processing	VLSI/2016
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102	JPV16102	Memory-Aware Loop Mapping on Coarse-Grained Reconfigurable Architectures	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
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104	JPV16104	An Efficient Single and Double-Adjacent Error Correcting Parallel Decoder for the (24,12) Extended Golay Code	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2016
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  - "SKR engineering college"
  - "Dr Pauls Engineering College"
  - "Jaya Engineering College"
  - "Jain College of Engineering"

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